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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,724	01/08/2007	Kozo Fujimoto	FUJIE396	3153
37013 7590 10/21/2008 ROSSI, KIMMS & McDOWELL, LLP. 20609 Gordon Park Square, Suite 150 Ashburn, VA 20147				
EXAMINER				
PATEL, DEVANG R				
ART UNIT		PAPER NUMBER		
1793				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/591,724

**Applicant(s)**

FUJIMOTO ET AL.

**Examiner**

DEVANG PATEL

**Art Unit**

1793

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 08 January 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SF/ICE)  
Paper No(s)/Mail Date 10/6/08, 6/3/08, 8/2/07, 10/27/06, 10/26/06, 9/5/06
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_



**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-5 and 7-9** are rejected under 35 U.S.C. 102(b) as being anticipated by Mikami et al. (JP 2002-110726 A).

a. **Regarding claim 1**, Mikami et al. ("**Mikami**") discloses an electronic part mounting method [figs. 1a-b] which joins circuit electrodes 2 which are made of metal and are formed over a circuit board 4 and die electrodes 2 which are made of metal and are formed over the electronic part 1 thus mounting the electronic parts on the circuit board, wherein a low-melting-point metal layer 3 is preliminarily formed over the circuit electrode and/or the die electrode and, thereafter, the circuit electrode and the die electrode are arranged to face each other, the circuit electrode and/or the die electrode are heated at a temperature which melts at least low-melting-point metal thus diffusing the low-melting-point metal layer into the circuit electrode and the die electrode by solid-liquid diffusion whereby the circuit electrode and the die electrode are joined to each other [¶ 85-86].

- b. **As to claim 2**, Mikami discloses that the low- melting-point metal layer contains at least one selected from a group consisting of Sn-In, In [¶ 32, 81].
- c. **As to claim 3**, Mikami discloses that a heating temperature at the time of the joining is a temperature which is 0 to 100°C higher than the melting point of the low-melting-point metal [¶ 86].
- d. **As to claim 4**, Mikami discloses a total thickness of the low-melting-point metal layer being 0.5 micron [¶ 85].
- e. **As to claim 5**, Mikami discloses that the material of the circuit electrodes and the die electrodes can be selected from a group consisting of Cu, Ni, or Au, [¶ 83].
- f. **As to claim 7**, Mikami discloses that the heating and the pressurizing are performed until the low- melting-point metal layer is completely diffused in the circuit electrode and the die electrode by solid-liquid diffusion [¶ 86-90].
- g. **As to claim 8**, Mikami discloses that the heating and the pressurizing are performed until an intermediate alloy layer 5 is formed between the circuit electrode and the die electrode [¶ 87].
- h. **As to claim 9**, Mikami discloses that the low-melting-point metal layer is formed such that at least two kinds of metals which can form alloy are stacked in two layers or more, and the stacked metal layers are preheated to make the metal layers react with each other to form an alloy layer ¶ 88-90].

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. **Claims 6 and 10-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Mikami et al. (JP 2002-110726 A) in view of Kimura et al. (US 5794839).

i. **As to claim 6**, Mikami discloses that the bonding surfaces are plastically deformed at the time of joining [¶ 18], but fails to expressly disclose a surface roughness of the bonding surfaces. However, **Kimura et al.** (drawn to bonding a semiconductor device) discloses that the surface roughness (Ra) of the bonding surface is related to the thickness of the bonding metal layer (In, Au-Sn etc.) and generally should be about one-third of the thickness [col. 7, lines 7-17]. Kimura further discloses the bonding metal layer having a thickness of 0.3-3 micron (similar to Mikami) for obtaining a high bonding strength [col. 7, line 37]. For instance, the surface roughness for a 3 micron thick layer would be about 1 micron (falls in the claimed range). It would have been obvious to one of ordinary skill in the art at the time of the invention to choose the instantly claimed roughness range through routine experimentation, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *See MPEP 2144.05*. Moreover, an artisan of ordinary skill would have been motivated to choose the claimed thickness and roughness ranges in order to achieve a high bonding strength [Kimura- col. 7, line 37].

j. **As to claims 10-11**, Mikami does not expressly disclose a vapor deposition process. However, such technique is well-known in the art of semiconductor bonding. **Kimura et al.** discloses forming a film of the solder alloy (evaporation source) by a vapor deposition process (physical or chemical), in which the composition ratio and the evaporation can be easily controlled [col. 5,

line 55- col. 6, line 20]. Kimura further discusses the dependence of the composition ratio on the vapor pressure of the alloy [col. 6, lines 25-38]. Kimura states that by forming a thin film by means of vapor growth, there is no excessive overflow of the solder, and a solder layer having a highly reproducible composition ratio can be obtained, thus a stable bond with high bonding strength is achieved [col. 6, lines 44-48]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to form the low melting point layer in the method of Mikami by vapor deposition of Kimura because such vapor deposition prevents excessive overflow of the solder, and produces a controlled, highly reproducible composition ratio and a stable bond with high bonding strength [Kimura- col. 5, line 56; col. 6, lines 44-48].

### ***Information Disclosure Statement***

The information disclosure statement (IDS) submitted on 10/6/08, 6/3/08, 8/20/07, 10/27/06, 10/26/06, 9/5/06 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Conclusion***

**Claims 1-11 are rejected.**

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Shibata (US 20020149117 A1), Akamatsu (US 5611481), Petitbon et al. (US 20020006685 A1), Wilde (DE 4303790 A1).



The rejections above rely on the references for all the teachings expressed in the text of the references and/or one of ordinary skill in the art would have reasonably understood from the texts. Only specific portions of the texts have been pointed out to emphasize certain aspects of the prior art, however, each reference as a whole should be reviewed in responding to the rejection, since other sections of the same reference and/or various combinations of the cited references may be relied on in future rejections in view of amendments.

Applicant is reminded to specifically point out the support for any amendments made to the disclosure. See 37 C.F.R. 1.121; 37 C.F.R. Part 41.37; and MPEP 714.02.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEVANG PATEL whose telephone number is (571)270-3636. The examiner can normally be reached on Monday thru Thursday, 8:00 am to 5:30 pm, EST..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jessica Ward can be reached on 571-272-1223. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. P./  
Examiner, Art Unit 1793

/Kiley Stoner/

Primary Examiner, Art Unit 1793